What is claimed is:

1. A field emission display (FED) with an integrated triode structure, comprising:

a substrate;

a cathode layer positioned on the substrate;

a gate insulating layer, which is positioned on the cathode layer and has a plurality of sub-microholes arranged in a regular pattern;

a gate electrode layer, which is positioned on the gate insulating layer and has a plurality of sub-microholes arranged in the substantially same pattern as that of the sub-microholes in the gate insulating layer;

an anode insulating layer, which is positioned on the gate electrode layer and has a plurality of sub-microholes arranged in the substantially same pattern as that of the sub-microholes in the gate insulating layer;

emitters, which are positioned in wells defined by the sub-microholes in the gate insulating layer, the gate electrode layer and the anode insulating layer, and the emitters being adhered to the cathode layer;

a phosphor layer positioned on the anode insulating layer; and

an anode layer positioned on the phosphor layer.

2. The FED with an integrated triode structure according to claim 1, wherein the FED further comprises a resistive layer which is positioned between the cathode layer and the gate insulating layer, and the emitters are adhered to the resistance layer.

3. The FED with an integrated triode structure according to claim 1, wherein the wells have a diameter of 4 to 500 nm.

4. The FED with an integrated triode structure according to claim 1, wherein the thickness of the anode insulating layer is in the

range of 100 nm to 10 μm.

5. The FED with an integrated triode structure according to claim 1, wherein the anode layer hermetically seals discharge spaces defined by the wells.

6. The FED with an integrated triode structure according to claim 1, further comprising a front plate which is positioned on the anode layer.

7. A method for manufacturing a FED with an integrated triode structure, the method comprising:

(a) forming, on a substrate, a cathode layer, a gate insulating layer, a gate electrode layer, and an aluminum layer, in order;

(b) converting the aluminum layer to an alumina layer using anodic oxidation, until the alumina layer has sub-microholes in a regular arrangement pattern and a barrier layer remained at the lower part of the sub-microholes;

(c) extending the depth of the sub-microholes in the alumina layer to the surface of the cathode layer;

(d) forming emitters in the sub-microholes, the emitters being adhered to the cathode layer;

(e) forming a phosphor layer on the alumina layer; and

(f) forming an anode layer on the phosphor layer under vacuum atmosphere.

8. The method according to claim 7, wherein step (a) further comprises forming a resistive layer on the cathode layer, in step (c), the depth of the sub-microholes is extended to the surface of the resistive layer and, and in step (d), the emitters are adhered to the resistive layer.

9. The method according to claim 7, wherein in step (b), the anodic oxidation comprises applying a positive voltage to the aluminum layer in aqueous solution of acidic electrolyte.

10. The method according to claim 9, wherein the acidic electrolyte is selected from the group consisting of oxalic acid, sulfuric acid, sulfonic acid, phosphoric acid, and chromic acid.

11. The method according to claim 7, wherein in step (b), the diameter of the sub-microholes is in the range of 4 to 500 nm.

12. The method according to claim 7, wherein step (c) is carried out using ion milling, dry etching, wet etching, or anodic oxidation.

13. The method according to claim 7, wherein in step (e), a phosphor is applied to the alumina layer using e-beam evaporation, thermal evaporation, sputtering, low-pressure chemical vapor deposition, sol-gel method, electroplating, or electroless plating.

14. The method according to claim 7, wherein the method further comprises increasing the diameter of the sub-microholes in the alumina layer by post-chemical treatment after step (b).

15. A method for manufacturing a FED with an integrated triode structure, the method comprising:

(a) forming, on a substrate, a cathode layer, a gate insulating layer, a gate electrode layer, an anode insulating layer and an aluminum layer, in order;

(b) converting the aluminum layer to an alumina layer using anodic oxidation, until the alumina layer has sub-microholes in a regular arrangement pattern and a barrier layer remained at the lower part of the

sub-microholes;

(c) extending the depth of the sub-microholes in the alumina layer to the surface of the cathode layer;

(c1) removing the alumina layers;

(d) forming emitters in the sub-microholes, the emitters being adhered to the cathode layer;

(e) forming a phosphor layer on the anode insulating layer; and

(f) forming an anode layer on the phosphor layer under vacuum atmosphere.

16. The method according to claim 15, wherein the anode insulation layer is formed of SiO_2, SiCOH, or insulating metal oxides.

17. The method according to claim 15, wherein step (c1) is carried out by dipping it in a solution of phosphoric acid or a mixed solution of phosphoric acid and chromic acid.

18. The method according to claim 15, wherein step (a) further comprises forming a resistive layer on the cathode layer, in step (c), the depth of the sub-microholes is extended to the surface of the resistive layer and, and in step (d), the emitters are adhered to the resistive layer.

19. The method according to claim 15, wherein the method further comprises increasing the diameter of the sub-microholes in the alumina layer by post-chemical treatment after step (b).